

MAX9850 Stereo Audio DAC with DirectDrive Headphone Amplifier

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REVISION A ERRATA

The errata listed below describe situations where the MAX9850 components perform differently than expected or differently than described in the data sheet (this Errata corresponds to Rev 1 of the MAX9850 data sheet). This errata sheet applies to all MAX9850 devices until further notice.

Description:

The MAX9850 data sheet states that the digital audio interface can operate in I²S mode in addition to left/right justified. After careful observation of actual part operation, it was found that data formatted using the I²S standard cannot be properly decoded by the MAX9850.

I²S is a "catch-all" term used to generically describe many digital audio interfaces. In reality, I²S is one of many digital audio formats that can be used to send digital audio data to a decoder. I²S is very similar to a mode Maxim calls "Left Justified." See Figures 1 and 2.

Figure 1 shows digital audio data left justified. This audio format is identified by the MSB of the data word on SDIN coinciding with the first BCLK transition after LRCLK changes state. Figure 1 shows left- and right-channel data both with the SDIN MSB being clocked in on the first BCLK rising edge after the LRCLK transition.

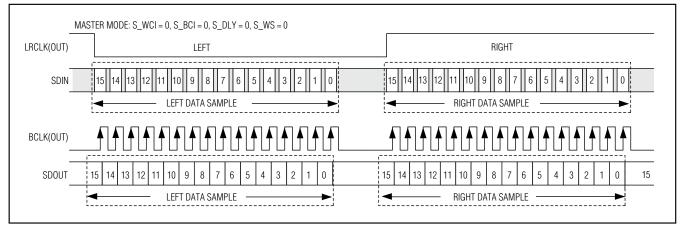


Figure 1. Left-Justified Audio Data

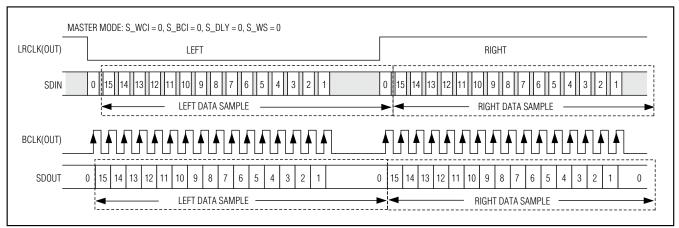


Figure 2. I²S-Formatted Digital Audio Data

Figure 2 shows digital audio data formatted using the I²S standard. I²S-formatted digital audio is identified by the MSB of the data word clocked into the decoder on the second BCLK pulse following an LRCLK transition. Figure 2 shows two channels of audio data being clocked into the decoder. Both channels have the MSB delayed by one BCLK cycle.

This delay is the main difference between I²S and left-justified digital audio formats.

Work Around:

Left-justified audio mode must be used instead of I²S mode.

Most $\mu P/\mu C/DSPs$ have a register(s) that controls how the digital audio data is formatted. The formats may not use the same naming convention as similar parts, but figures showing the data timing or frame format can be used to determine which mode needs to be used for proper MAX9850 operation.

For example, the Freescale SCF5250 microprocessor uses a digital audio interface that can operate in two modes. They call these modes IIS (I²S) mode and Sony EIAJ mode (left justified).

The user's manual for the part can be found here

http://www.freescale.com/files/platforms/doc/user_guide/SCF5250_USERS_MANUAL.pdf

Page 17-5 details the three digital audio interface registers. Tables 17-4 to 17-7 detail the configuration registers and bit descriptions.

The bit named MODE (bit 5) allows the user to toggle between the two modes.

Figure 17-2 on page 17-10 is a graphical representation of the two modes (IIS and EIAJ). This figure can be used to compare the format to the MAX9850 data sheet to see that EIAJ mode (from the Freescale data sheet) and left-justified mode (from the MAX9850 data sheet) are the same.